CLAIMS

1. A method for finding the boundary between words in a stream of data bits, each data bit defining a bit cycle, the method comprising the steps of:

defining a high and a low logic level;

determining the sequence of bits defining a word;

selecting a data signal defining a word boundary;

adding the word boundary with the bits defining the word;

sending out in serial form the word data bits with the added word boundary;

sending out in parallel with the data bits, a bit clock synchronized with the data bits;

causing the bit clock to maintain a constant logic level during the sending of the word boundary; and

determining the word boundary by sensing the word boundary while the bit clock maintains a constant logic level.

2. The method of claim 1 wherein the step of selecting the boundary comprises the step of creating logic level transitions at a double bit cycle frequency during a bit cycle, the double bit cycle during a bit cycle defining the word boundary.

3. The method of claim 1 wherein the step of determining a word boundary comprises the step of:

selecting two added boundary data bits, the data bits having the same bit cycle as the data bits, the boundary data bits selected so that there is a logic level transition at the beginning of the first boundary bit and at the junction of the two added boundary data bits.

4. The method of claim 1 wherein the clock logic level remains high during a word boundary.

5. The method of claim 1 wherein the clock logic level remains low during a word boundary.

6. The method of claim 3 wherein the logic level transition at the junction of the two boundary bits is from low to high.

7. The method of claim 3 wherein the logic level transition at the junction of the two boundary bits is from high to low.

8. The method of claim 1 further comprising the steps of placing filler bits before and after the data word and word boundary.

9. The method of claim 1 wherein the word boundary is placed within the word data bits.

10. The method of claim 1 wherein the word boundary is placed before the word data bits.

11. The method of claim 1 wherein the word boundary is placed after the word data bits.

12. The method of claim 3 further comprising the steps of:
loading a parallel data word into a shift register;
defining the word boundary as bits sharing the same bit cycle as the word data bits;
loading the word boundary bits into the shift register;
shifting out the word data bits and the word boundary bits; and
loading the next parallel data word and word boundary bits into the shift register.

13. The method of claim 1 further comprising the steps of:

defining the word boundary as bits sharing the same bit cycle as the word data bits;

receiving the serial word data bits and the word boundary bits;

receiving the synchronous bit clock;

shifting the received word data bits and the word boundary bits, bit by bit, into a shift register using the received synchronous bit clock;

detecting when a data word has been shifted into the shift register, and in response indicating the receipt of the word to a computing system; and

reading the word by the computing system.

14. Apparatus for finding the boundary between words in a stream of data bits, each data bit defining a bit cycle, the apparatus comprising:

means for defining a high and a low logic level;

means for determining the sequence of bits defining a word;

means for selecting a data signal defining a word boundary;

means for adding the word boundary with the bits defining the word;

means for sending out in serial form the word data bits with the added word boundary;

means for sending out in parallel with the data bits, a bit clock synchronized with the data bits;

means for causing the bit clock to maintain a constant logic level during the sending of the word boundary; and

means for determining the word boundary by sensing the word boundary while the bit clock maintains a constant logic level.

15. The apparatus of claim 14 wherein the means for selecting the data signal defining a word boundary comprises means for creating logic level transitions at a double bit cycle frequency during a bit cycle, the double bit cycle during a bit cycle defining the word boundary.

16. The apparatus of claim 14 wherein the means for determining a word boundary comprises:

means for selecting two added boundary data bits having the same bit cycle as the data bits, the boundary data bits selected so that there is a logic level transition at the junction of the two added boundary data bits.

17. The apparatus of claim 14 wherein the clock logic level remains high during a word boundary.

18. The apparatus of claim 14 wherein the clock logic level remains low during a word boundary.

19. The apparatus of claim 14 wherein the logic level transition at the junction of the two boundary bits is from low to high.

20. The apparatus of claim 14 wherein the logic level transition at the junction of the two boundary bits is from high to low.

21. The apparatus of claim 14 further comprising means for placing filler bits before and after the data word and word boundary.

22. The apparatus of claim 14 wherein the word boundary is placed within the word data bits.

23. The apparatus of claim 14 wherein the word boundary is placed before the word data bits.

24. The apparatus of claim 14 wherein the word boundary is placed after the word data bits.

25. The apparatus of claim 17 further comprising:

means for loading a parallel data word into a shift register;

means for defining the word boundary as bits sharing the same bit cycle as the word data bits;

means for loading the word boundary bits into the shift register;

means for shifting out the word data bits and the word boundary bits; and

means for loading the next parallel data word and word boundary bits into the shift register.

26. The apparatus of claim 14 further comprising:

means for defining the word boundary as bits sharing the same bit cycle as the word data bits;

means for receiving the serial word data bits and the word boundary bits;

means for receiving the synchronous bit clock;

means for shifting the received word data bits and the word boundary bits, bit by bit, into a shift register using the received synchronous bit clock;

means for detecting when a data word has been shifted into the shift register, and in response;

means for indicating the receipt of the word to a computing system; and

means for reading the word by the computing system.